A Feedforward Third-Order Tri-Level Oversampling ADC

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ABSTRACT

This paper presents a high resolution third-order tri-level cascade of multiple feedforward (CIFF) delta sigma modulator analog to digital Converter (ADC). The modulator is target for moderate to higher bandwidth applications. Due to CIFF topology the signal transfer function (STF) of the modulator will have peaking effect. While the NTF of the modulator shows ideal noise shaping as the amplifier are considered infinite DC gain. The key performance parameters of the modulator are investigated like out of band gain (OBG), full scale and NTF zero optimization technique. Due to higher order of the loop filter the out of band-gain (OBG) of the modulator kept smaller. The full-scale of the modulator raised until the stability of the modulator becomes challenge. To further enhance the performance of the modulator NTF zero optimization techniques is implemented, that enhance the SNR of 6dB. The integrators inside the loop filter are optimized limited DC gain, confined slew-rate, and unity gain bandwidth. The suggested structure allows to use single feedback digital-to-analog (DAC). Which simplifies the topology but also imposes challenge for the stability of the modulator. Also due to multiple feedforward topology the operational amplifier inside the loop filter does not requires very high DC gain as loop filter only process quantization noise as signal is feedforwarded to the quantizer. The CIFF modulator with OSR of 128 can achieve signal to noise ratio of 120 dB for signal bandwidth of 100 kHz.

Keywords: Full-scale input, Operational amplifier, out-of-band gain, Signal transfer function, Noise transfer function

1. INTRODUCTION

Analog front-end are challenging to design and interface and constraints the power consumption as it needs to be integrated with other building blocks. A feedforward third-order tri-level oversampling ADC is modeled and simulated for moderate to higher bandwidth application. The modulator performance parameters OBG, full-scale and NTF zero optimization techniques discussed. The oversampling analog to digital converter is a commonly used component in a variety of applications, including audio and instrumentation. Delta sigma modulators (DSMs), which use dual oversampling and noise shaping capabilities, have proven to be a good option for low to medium bandwidth high resolution converters. The fundamental disadvantage of an oversampled technology is that the signal bandwidth is limited to a small percentage of the total bandwidth. As demand for data conversion interfaces with digital systems grows for reasons of cost, flexibility, and stability, supply voltage decrease and lower transistor intrinsic gain pose substantial difficulties to data interface architecture, one of the most crucial mixed signal tasks. When the dynamic range is limited by thermal noise, a lower supply voltage decreases the available signal swing , that often enhances the analog power consumption required to accomplish a certain dynamic range. Furthermore, due to the restricted voltage headroom, a

lowered supply voltage limits the circuit topologies that can be used. Designing high precision analog circuits, which performance is sometimes dependent on the quality of the virtual grounds, is made more difficult by decreased transistor inherent gain. Either the sampling frequency or the order of the modulator should be raised to improve the signal bandwidth while retaining the signal to quantization noise ratio (SQNR) and the number of back end quantization levels. Enhanced power consumption is associated with higher sampling frequency, and enhanced noise shaping order is associated with worries about stability. The creation of a 1 V ADC with minimal power consumption has recently received a lot of attention. To begin with, the supply voltage of advanced CMOS technology decreases as the size of the device feature increases. Low supply voltage restricts voltage headroom, therefore for a given dynamic range (DR) requirements, more power is generally required. Second, MOS transistors' intrinsic gain is drastically reduced. The intrinsic gain of devices with a 65 nm process is said to be 80% smaller than that of devices with a 130 nm method. Low internal gain results in low amplifier gain, which has an impact on analog to digital converter correctness. Third, in order to save energy, low power circuitry is in high demand in electronic products. Delta sigma modulators come in a variety of topologies. The cascade of integrators with multiple feedback is the first, while the cascade of integrators with multiple feedforward CIFF is the second. The feedforward approach has the benefit of not having a signal component at the integrator output, and the integrators simply processes the quantization error. As a result, the integrators' voltage swings are decreased. The quantization step is reduced by using a 3-bit quantizer, and swings are reduced even more. The feedforward path has a half second delay, which allows the quantizer's timing requirements to be relaxed. The modulator's characteristic, which will be discussed later, is unaffected by such a delay. The amplifier's gain need is relaxed when the swings are reduced. The integrator can be built using a simple amplifier such as a single stage amplifier or even an inverter based amplifier, which saves power. To improve amplifier gain at low voltage without this characteristic, the cascaded approach must be used. For two reasons, more power is needed. For starters, the power rail and ground have additional branches. Second, in order to ensure amplifier stability in a feedback setup, a significant current is needed to push additional poles associated with cascaded stages far away [1]. Because wideband applications have a low oversampling ratio and the quantizer has a limited number of bits, the demand for high resolution can be fulfilled by obtaining more aggressive noise shaping in delta sigma modulator. As the order of the loop modulator rises, it is more likely to become unstable. To stabilize the high order modulator, the out of band gain (OBG) must be decreased at the cost of increased quantization noise and circuit complexities due to additional coefficient routes. Another option for dealing with the stability issue is to use a Multi stage Noise Shaping delta sigma modulator, which consists of many inherently stable low-order single loop modulators cascaded together [2]. The MASH modulator, however, are more stable because they use cascaded low order modulator loops to improve noise shaping. However, high accuracy analogue component are required to reduce quantization noise leakage due to the matched requirement between analog loop filters and digital transfer functions.

This necessitates the use of highly precise integrators/operational amplifiers, as well as modulator coefficients. Furthermore, in low voltage applications, a high operational amplifier gain need necessitates a multi stage operational amplifier, limiting total efficiency to both stability and power consumption [3].

This paper proposed a high resolution third-order tri-level CIFF delta sigma modulator. The modulator is target for moderate to higher bandwidth applications. Due to CIFF topology the signal transfer function (STF) of the modulator will have peaking effect. While NTF of the modulator shows ideal noise shaping as the amplifier are considered infinite DC gain. The key performance parameters of the modulator are investigated like out-of-band gain (OBG), full-scale and NTF zero optimization technique. Due to higher order of the loop filter the out of band gain (OBG) of the modulator kept smaller. The full-scale of the modulator raised until the stability of the modulator becomes challenge. To further enhance the performance of the modulator NTF zero optimization techniques is implemented, that enhance the SNR of 6dB. The integrators inside the loop filter are optimized limited DC gain, restricted slew-rate, and unity gain bandwidth. The proposed structure allows to use single feedback digital-to-analog (DAC). Which simplifies the topology but also imposes challenge for the stability of the modulator. The CIFF modulator with OSR of 128 can achieve Signal to noise ratio of 120 dB for signal bandwidth of 100 kHz.

After the introduction, the second section discuss the design of the modulator design with CIFF topology, while the third section describes the modeling and simulation of the modulator and explain the role of high performance operational amplifier for integrator in the third-order multi-bit modulator. Finally, the section four concludes the paper.

2. MODULATOR DESIGN

A third-order multi-bit modulator modeled using Delta-Sigma Toolbox [8]. The cascade of integrator with multiple feedforward (CIFF) allows much smaller swing inside the loop filter due to multiple feedforwarded signals. Also, the noise transfer function (NTF) shows very smooth noise shaping performance. While the signal-transfer-function (STF) causes shows peaking effect rather than completely smooth response as shown in

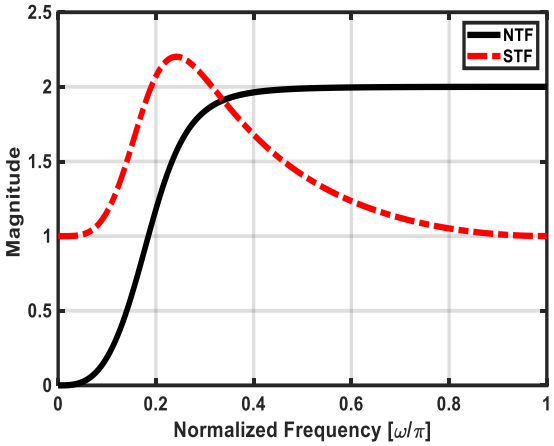

Figure 1: STF and NTF plot (CIFF)

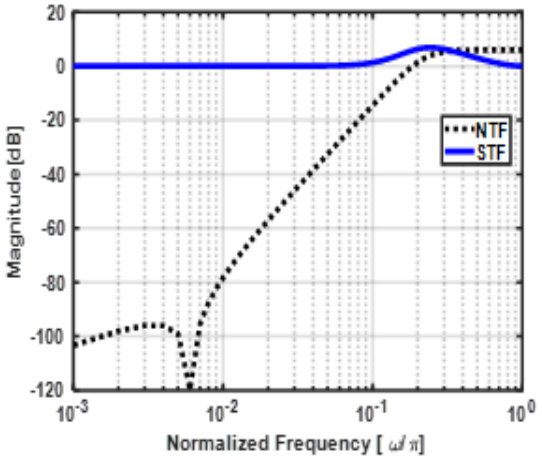

Figure 2: STF and NTF plot (CIFF)

Figure. 1. The NTF zero optimization causes more in-band quantization noise shaped to out-of-band and results in improved performance. The CIFF modulator coefficient obtained from the toolbox shown in Table-I. These coefficients represent the ratio of capacitors at the switched-capacitor implementation, for the discrete-time implementation of the modulator. Those coefficients which are not mentioned, have value zero. The Table II shows the Full-scale comparison of the proposed modulator CIFF topology. With three integrators inside the loopfilter the smaller full-scale results in smaller SNR performance. While larger full-scale results in higher SNR performance. The Table III shows the comparison of OBG and SNR, OBG plays a very important influence in modulator efficiency. The Figure .2 shows the STF and NTF plot of the CIFF third order CIFF topology. Due to ideal integrators with NTF zeroes at DC, the slope is 60dB/decade. The output states of the integrator are shown in the Figure 3. Due to the CIFF topology the swing inside the loop filter is very smaller and requires low DC gain amplifier for the integrators. All operational amplifier inside the loop filter is ideal have infinite gain to suppress the quantization noise in the signal band of the modulator.

Table I : CIFF Cofficients

Parameters	Values
a_1	1.33
a_2	0.741
a_3	0.161
b_1	1
g_1	0.000361
c_1	1
c_2	1
c_3	1

Table II: Full Scale Comparison

Full Scale	SNR
0.1 volt	106
0.2 volt	111
0.3 volt	116
0.4 volt	120

Table III : OBG vs SNR

OBG	SNR
1.1	94
1.3	107
1.5	112
2	120
2.2	123
2.5	125
3	128

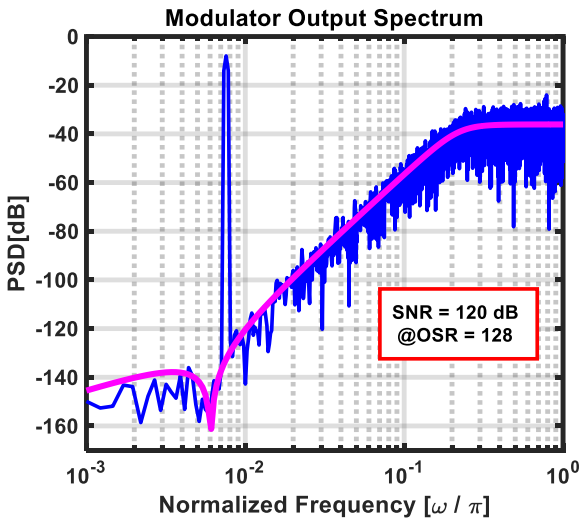

Figure 3: Output PSD plot (CIFF)

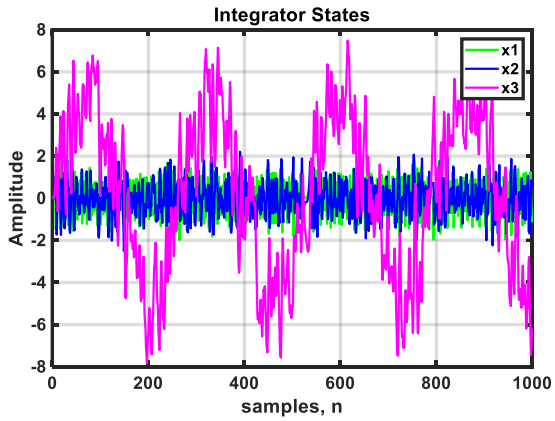

Figure 4: Output states of the integrators

3. NON-IDEALITIES SIMULATION

The feedforward modulator topology investigated for moderate to higher bandwidth application in MATLAB. With an OSR of 128 and a signal bandwidth of 100 kHz, the modulator can obtain an SNR of 120 dB. To realize the practical implementation of the modulator, non-idealities need to be simulated so that circuit designed can get an estimate of the performance. The simulation environment SDToolbox [10] which simulates the circuit non-idealities are used. This section will discuss about the circuit non-idealities like thermal noise or kT/C, flicker noise, finite operational amplifier gain, finite slew-rate, finite gain-bandwidth (GBW).

4. CONCLUSION

A CIFF topology modulator can obtain higher SNR of 120 dB for signal bandwidth of 100 kHz. The CIFF topology different design parameter investigated for higher performance. Due to ideal modeling of the modulator the NTF zeroes lies at the DC for optimum suppression of quantization noise.

5. ACKNOWLEDGMENT

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