Design of 62-dB DC Gain Two-Stage CMOS Operational Amplifier

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ABSTRACT

This work presents two-stage operational amplifier based on CMOS technology, which operates at given input of 1-V power supply using the 180nm CMOS technology and whose input is depend on different Biasing voltage. To reduce supply voltage and obtain the high voltage gain is main objective of operational amplifier. The digital circuits have more accuracy of size reduction and given input supply voltage while the other side analog circuits is based on different parameters like noise, gain, power consumption and bandwidth for best performance. This paper present the two stage operational amplifier designed in 180nm CMOS technology with 62.07dB AC gain and phase margin of 65° with unity gain frequency of 1.54-MHz. This work consume the power of 131uW.

Key words: CMOC, Op-amp, Noise, Gain, Power

1. INTRODUCTION:

The mention work present the detail of designing and performance parameter of two stage operational amplifier.

Operational amplifier is basic building block for designing all analog side area and mixed signal system. Op-amp is a linear device and almost found all the specification, which needed to all amplification for DC, and many other operations [1]. For high-speed operation, the telescopic architecture is always preferable. This two-stage operational amplifier designed in double Cascode telescopic input in the first stage to obtain high gain and the common source amplifier used the second stage of op-amp [6]. The input is execute on NMOS or PMOS transistors. The maximum stability of NMOS devices provide a maximum gain [9].

These operational amplifiers are commonly allocates, for high gain and offers good bandwidth with less power consumptions.

The mention architecture of operational amplifier consume the less power of 131uW with best performance. With suitable phase margin, bandwidth, maximum gain in minimum power the Op-amp needed to biomedical and many other areas [7].

I show there the slew rate of operational amplifier with I_{tail}/C_L where the I_{tail} and C_L are the current and load capacitance of the operational amplifier [2].

Symbol diagram of operational amplifier is describe in Fig 1 with differential two input and two output.

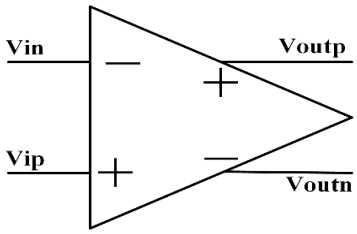

Fig 1 Symbol of Differential op-amp

The paper organized in different section. Where the section 2 describe about the

system architecture. Section 3 present specification of op-amp. Section 4 provides the performance of architecture. Finally, our result is given in section 5 and references in 6.

2. ARCHITECTURE OF OP-AMP

The schematic of the first and second stage of the designed operational amplifier is given in fig.2. The single stage op-amp comprises of PMOS transistor M1-M4 and NMOS of M5 to the tail transistor of M9. This circuit consist of two inputs, which are differential based, and a common source is followed at the second stage. The differential based input is used to provide the gain at the initial stage, while to increase the gain by an order of magnitude and maximizes the output swing, second stage is used. It is important to note that voltage reduction across the tail transistor has the quality of improvement in differential swing as the tail transistor cuts into the output swing from both sides of the amplified [5].

To increase the phase margin, compensation is one method applied[3]. The capacitor is used for compensation that is connected in second stage between the input and output that causes to split apart the poles associated with them. Transistor M7 and M8 are as the input transistors while the output to the second stage sets the drain voltage of M3 and M4 in the main amplifier. Here the fig.2 describe the detail implementation of operational amplifier.

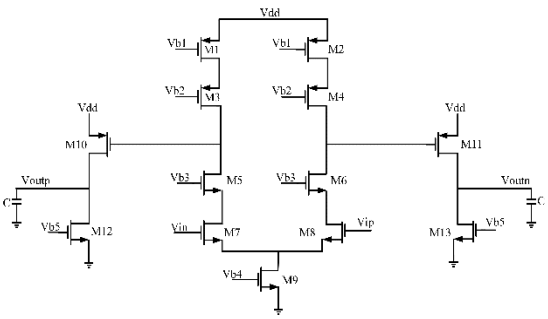

Fig 2. Architecture of Op-Amp

3. SPECIFICATION OF OP-AMP

Proposed design parameter are given in table 1. This reflection is used to describe the length and its width of transistor which schematic shown in fig2. For high speed operation the telescopic operational amplifier is always preferable, however the telescopic op-amp usually required large power supply [8]. Below table, no 1 is the detail specification of op-amp.

Table no 1. Specification of Op-amp

Transistor	W/L	Current
M1, M2	21µm/180nm	65µA
M3, M4	18µm/180nm	65µA
M5, M6	10um/180nm	65µA
M7, M8	6µm/180nm	65µA
M9	12µm/180nm	130µA
M10, M11	12µm/180nm	129nA
M12, M13	220nm/180nm	129nA

4. PERFORMANCE PARAMETER

Given performance parameter of op-amp describe in below table no 2. With given supply voltage of 1-V it achieve the best performance of AC gain with phase margin of 65° and less power dissipation of 131uW. Op-amp with best performance parameter is challenging and will be used in many more.

Table no 2: OP-Amp Specification

Parameter	Specification
DC Gain	62.07dB
Phase Margin	65°
Unity Gain Frequency	1.54 MHz
Vdd	1-V
Power Dissipation	131uW

5. SIMULATION RESULT

This part of the paper discusses the simulation result of the two stage telescopic operational amplifier. The

operational amplifier have the simulation performance of transient analysis, AC gain, slew rate, phase margin and their power consumption. All these performance are varied using the 180 CMOS Nano-technology with 1-V supply voltage. The output of operational amplifier has high linearity for high currents. This does not require any additional circuit [4]. Gain and phase margin of operational amplifier are given in below fig 3.

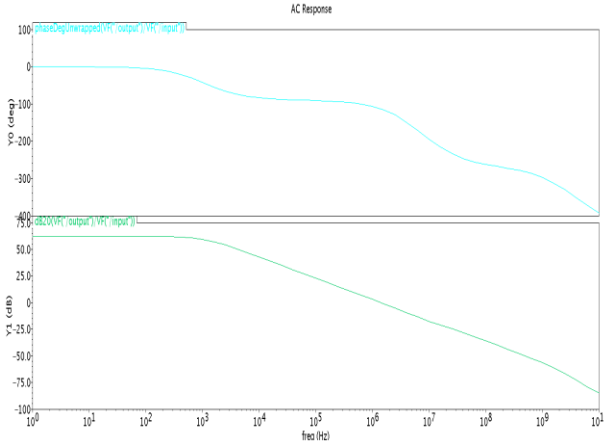

Fig 3. Gain and Phase of Op-Amp

6. CONCLUSION

From two-stage op-amp, to get optimized performance the various factors taken into consideration while designing the architecture. This paper is two-stage Op-amp architecture design in 180nm CMOS based technology. This Design of architecture is made through the scaling of devices parameter. The architecture and the circuit issue were discussed.

7. REFERENCES

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